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INVENTOR(S)

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☐ *Additional inventors are being named on the ____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

SIGMA DELTA MODULATOR

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Respectfully submitted,

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Sigma Delta Modulator

Field of the invention

The present invention relates to a sigma delta modulator. More particularly, to a sigma delta modulator where the transfer function of a loop filter is shaped to adapt performance of the sigma delta modulator to different signal amplitudes.

Background

In recent years so-called sigma delta converters have become very popular to use in A/D or D/A converters, but they are also applied in different types of Class-D amplifiers both in analogue and digital implementations. Further the so called band-pass sigma delta converters have also been discussed in the literature, this kind of converter is especially useful for the up/down modulation in combination with digital/analogue conversion of the RF base-band signals used in modern digital wireless communications system. As sigma delta modulators are compatible with modern CMOS technology and does not require any special and expensive features it has become very popular and there exists many more applications than mentioned here.

Generally, it is necessary to sample a signal at a sampling frequency greater than or equal to the Nyquist frequency to be able to reproduce the signal without loss of information. Therefore the vast majority of converters operate at sampling frequencies closely related to the Nyquist frequency. The amplitude of the signal is resolved in a number of discrete steps as determined by the A/D or D/A converter.

Conventional converters are build around a quantizer with a relatively fine resolution typically specified by the number of bits with which the signal is represented e.g. 8 bits, 12 bits or 16 bits. Due to the fine resolution of the quantizer complexity of the converter will go up dramatically when the

resolution of the converter is increased and cost of the converter will go up when the sampling frequency is increased.

However, sigma delta converters are build around a quantizer with a relatively coarse resolution of typically 2, 3 or 4 levels. This low resolution quantizer can be operated at a greater sampling frequency than the fine resolution quantizer, but at the cost of it producing a larger quantization error ie the difference between the input signal and the output signal. To compensate for this larger quantization error, the sigma delta modulator is based on a feedback loop where a quantization error value produced by the quantizer in a sampling time instance is subtracted from a signal value input to the quantizer in a subsequent sampling time instance. Thereby, the error signal is integrated to provide a signal which in average has no error.

A bit stream at the greater sampling frequency is generated. Since typically it is inconvenient to perform subsequent signal processing at the greater sampling frequency, a decimation process is applied to the bit stream whereby a digital output signal at a rate of about the Nyquest frequency and with a desired relatively fine resolution is provided. Generally, the sigma delta modulator provides lower distortion and lower cost when compared to conventional converters.

Fig. 1 shows a model of a generic sigma delta modulator. The sigma delta modulator is shown in a discrete time domain implementation where x(n) and y(n) are an input signal and an output signal, respectively, with signal values at discrete time instances n. The modulator comprises an input filter, G(z), a quantizer, Q(z), a loop filter, H(z), and an adder, A.

Due to the integrator function of the feed-back loop the sigma delta converter acts as a low-pass filter for an input signal and as a high-pass filter for the quantization noise. This is an expedient behaviour in that when the loop filter

is designed to pass input signals in a signal band, quantization noise is attenuated in that signal band.

The noise attenuation is appreciable even with a first-order sigma delta modulator, that is, a modulator comprising a single integrator upstream of the quantizer, but to achieve the high signal/noise ratios required of high resolution converters, it is necessary to use higher-order modulators, that is, modulators comprising several integrators in cascade. However, if a higher-order modulator is used, stability problems arise.

In the design of the sigma delta converter it's an objective to minimize the quantization noise in the pass-band produced by the quantizer Q(z) i.e. to modulate the quantization noise. Further it's a objective to maximize the maximum stable amplitude, usually denoted MSA, swing of the modulator as this determines the maximum input signal one can apply to the modulator.

Both these objective will maximize the dynamic range of the modulator and the last objective are especially useful in Class D converters and in low voltage implementation of the modulator. A Third objective is to minimize the die size and power consumption of the modulator in an ASIC implementation.

Unfortunately these above three objectives are partly conflicting, and a compromise has to be made i.e. a trade off exist between minimizing the quantization noise (in the pass-band) and obtain high MSA and so on. Usually the optimum, taken all three objective into consideration, ends up with a MSA around 0.5 (or 6 dB below full-scale). See for example the DSD1702 data sheet from Texas Instrument where a sigma delta modulator is used in a D/A converter.

Prior art

US 2002/0030618-A1 discloses a method of re-establishing the stability of a sigma delta modulator and a circuit for implementing the method.

Generally, this prior art document is concerned with the issue of re-establishing stability since in a higher order sigma delta modulator lack of stability will destroy performance of the modulator. Thus the prior art is focused on finding solutions in which signals that indicate a state of lack of stability is detected to bring the modulator back into a stable state to revive performance of the sigma delta modulator.

However, a modulator according to such prior art will suffer from a dominant or relatively high Total Harmonic Distortion, THD, due to abrupt or highly non-linear control of the sigma delta modulator.

Summary of the invention

The present invention provides a method of controlling a sigma delta converter whereby the trade-off between MSA and noise suppression in the pass-band is eliminated by controlling the Noise Transfer Function.

In one aspect the invention relates to a method of controlling a sigma delta modulator with a loop filter that establishes a signal transfer function and a quantization noise transfer function of the sigma delta modulator; the method comprises the step adaptively shaping the quantization noise transfer function in response to a value of a signal feature.

Thereby quantization noise is shaped to allow gradual levels of quantization noise in a frequency band of interest by adapting the coefficients of a loop filter and thus the quantization noise transfer function in response to the value of the signal feature.

Preferably, when the measured value represents a relatively large amplitude, the noise transfer function is shaped to suppress quantization noise to a less extent relative to when the measured value represents a relatively low amplitude, the noise transfer function is shaped to suppress quantization noise to a larger extent.

Preferably, it is evaluated at a sampling rate whether to apply the step of shaping the quantization noise transfer function. Due to the relatively high sampling rates of sigma delta modulators, the sampling rate in an audio application can be e.g. 2.4 MHz or lower or higher.

It is possible to shape of the quantization noise by moving zeroes or poles in the transfer function and/or by adjusting loss coefficients in the transfer function. Or by adjusting the resolution and or the thresholds of the quantizer.

Preferably, the signal feature is a rectified peak value of the input signal.

Preferably, filter coefficients are pre-computed and stored in a loop-up table. Therefore a method of the invention can comprise the step of computing coexisting values of amplitude ranges, MSA, and loop filter parameters, which are coexisting in the sense that for a given value of an amplitude range, the coexisting loop filter parameters, when applied in the loop filter, provide a modulator which is stable for signal amplitudes less than the given value of an amplitude range.

The invention is typically embodied as a segment of a sigma delta converter that controls the loop filter in response to a signal feature calculated from a signal in the sigma delta converter. Typically, the loop filter comprises a cascade of filter stages. The implementation of the loop filter or the modulator can be either a digital implementation or an analogue implementation, with e.g. a switched-capacitor filter, an RC-filter implementation, or a mixed

analogue/digital implementation. In general the loop-filter can be implemented in many ways and in different domains. There exists mathematical transformations which transform any implementation into a time discrete implementation and thus all the design procedures and the invention described herein can be utilized in many different implementations; e.g. a transformation exists from band-pass modulators to low-pass modulators and vice versa. From continuous time to discrete time etc.

The noise transfer function is determined by the loop filter of the sigma delta modulator. For a given noise transfer function an MSA value can be estimated. A noise transfer function is selected such that the MSA value of the noise transfer function adapts to the amplitude of an input signal e.g. a peak value of the input signal.

The current invention makes it possible to obtain Full Scale output swing even for high orders modulators and still maintain a good quantization noise rejection for lower signal input. By using this invention in high order modulators dynamic range is extended up to 6 dB or more.

Brief description of the drawing

The invention will be described in connection with the drawing in which:

fig. 1 shows a model of a generic sigma delta modulator;

fig. 2 shows a model of the generic sigma delta modulator with a linearized quantizer;

fig. 3 shows a example of a noise transfer function and a signal transfer function of a 4'th order sigma delta converter;

fig. 4 shows two different curves for the noise amplification factor A as a function of a linearized quantizer amplification factor Kn;

fig. 5 shows a curve for the noise amplification factor A as a function of a signal peak value m_x for a Gaussian distributed quantizer input signal;

fig. 6 shows a relation between A(Kn) and A(m_x), quantizer gain Kn and a stable input range, MSA;

fig. 7a shows a sigma delta modulator with a control circuit that controls the noise transfer function and the signal transfer function of the modulator;

fig. 7b shows a sigma delta modulator with a control circuit which receives an input signal of the modulator;

fig. 8a shows the element of the generic control circuit, called the NSCTR, of the invention;

fig. 8b shows a preferred embodiment of the NSCTR;

fig 8c shows another preferred embodiment of the NSCTR;

fig. 9 shows a block diagram of the sigma delta converter according to the invention;

fig. 10a and 10b show block diagrams of the integrator $H_i(z)$ of the modulator in fig. 9;

fig. 11 shows a first set of noise transfer functions that provides different MSA values and different quantization noise attenuation;

fig. 12 shows a second set of noise transfer functions that provides different MSA values and different quantization noise attenuation;

fig. 13 shows a third set of noise transfer functions that provides different MSA values and different quantization noise attenuation;

fig. 14 shows a fourth set of noise transfer functions that provides different MSA values and different quantization noise attenuation;

fig. 15 shows another preferred embodiment of the sigma delta converter according to the invention when implemented as a digital modulator;

fig. 16a and 16b show block diagrams of the integrator $H_i(z)$ of the modulator in fig. 15;

fig. 17 shows a further preferred embodiment of the sigma delta converter according to the invention when implemented as a digital modulator;

fig. 18a shows a range of required MSA for a given input signal peak value to provide stable operating conditions;

fig. 18b shows a realized MSA as a function of a input signal peak value, mx, for an exemplary design in which the MSA can be adapted to the peak value by selecting of one of five different noise transfer functions;

fig. 19 shows different noise levels in a frequency band of interest;

fig. 20 shows a class-D amplifier comprising a sigma delta modulator and a so-called H-bridge arranged to drive a load;

fig. 21 shows a configuration of an H-bridge;

fig. 22 shows a first embodiment of a digital microphone with a sigma delta converter;

fig. 23 shows a second embodiment of a digital microphone with a sigma delta converter;

fig. 24 shows a first block diagram of a digital microphone;

fig. 25 shows a second block diagram of a digital microphone;

fig. 26 shows a schematic view of a microphone with an integrated circuit and a microphone member.

Detailed description of a preferred embodiment

In order to explain the invention some common phrases has to be introduced and a summery of a model of the sigma delta modulator that is commonly used will be given.

Fig. 2 shows a model of the sigma delta modulator with a linearized quantizer. The sigma delta modulator is shown in a discrete time domain implementation where x(n) and y(n) are an input signal and an output signal, respectively, with signal values at discrete time instances n. The modulator comprises an input filter, G(z), a quantizer, Q(z), a loop filter, H(z), and an adder, S1.

The most common way to analyze the a sigma delta modulator is to replace the highly nonlinear quantizer Q(z) with a linearized quantizer in the form of an amplifier A1 with a gain factor, *Kn*, designated quantizer gain and a noise

source designated q(n). The noise source contributes to the output of the quantizer via an adder, S2. *Kn* and q(n) comprises values at discrete time instances n. It should be noted that kn changes very slowly compared to the rate of the clock frequency.

In this description a model in the Z-domain is used, which can be used for both analogue switch capacitor implementation and a digital implementation of the modulator. This Z-domain description can be transformed to a continuous time domain description to provide an RC modulator implementation.

It should be noted that the conventional theory on linear system cannot be used to analyze the modulator due to the high nonlinear quantizer, this is very well described in the sigma delta modulator literature. However, by means of the linearized model the signal transfer function, STF, and the noise transfer function, NTF, are found to be (please refer to the common literature):

$$STF_{Kn}(z) = \frac{Y(z)}{X(z)} = \frac{K_n G(z)}{1 + K_n H(z)}$$

$$NTF_{Kn}(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1 + K_n H(z)}$$

These are the functions that will describe the behaviour of the transfer from the input, x, to the output y and from the noise source, q, to the output, y, respectively. In order to simplify the analysis or design of the loop filter G(z) can be set equal to H(z).

If the filter, H(z) is designed as a M'th order low-pass filter then the STF will be an M'th order low-pass filter and the NTF will be an M'th order high pass

filter and the order of the modulator is said to be of M'th order. If H(z) is designed as a band-pass filter then the STF and NTF becomes a band-pass filter and a band-stop filter, respectively. These filters are especially expedient for modern digital communications system.

Fig. 3 shows an example of the noise transfer function, NTF, and the signal transfer function, STF, of a 4th order sigma delta converter. The transfer functions are shown as gain versus frequency, f, normalised by the sampling frequency, fs. The NTF is shown with a fixed *Kn* for e.g. a 4'th order Butterworth high-pass characteristic. The characteristic is obtained by means of a loop filter with a 4th order Butterworth low-pass filter. However, other types of filter could be used e.g. a Chebycev filter. As a consequence, the loop filter establish a signal transfer function, STF, which has a pass-band where the noise transfer function has its stop-band and vice versa.

Hence, the noise attenuation of the high-pass filter, NTF, in its stop-band determines the noise level in the pass-band of the low-pass filter, STF.

As a design parameter a 'nominal frequency band' or a 'frequency band of interest' designates a frequency band in which input signals can occur and which it is desired to pass through the sigma delta modulator.

For a conventional sigma delta modulator the loop filter is designed such that signal transfer function implements a desired 'nominal frequency band' or 'frequency band of interest'. In the shown STF and NTF the frequency band below normalised frequencies $f_{c,Bol}$ is the frequency band of interest.

According to the invention the noise transfer function, NTF, is shaped in response to a signal amplitude value in the sigma delta modulator. This shaping can result in the pass-band of the signal transfer function being

changed. In most cases though, the changes of the STF will be well above the band of interest and thus of no concern.

The better attenuation in the stop-band of the NTF means the quantization noise contribution will be lower however as discussed in the following the MSA for a conventional modulator will decrease.

The STF and NTF are the functions that determine the signal properties of a sigma delta converter and the basic idea of a sigma delta converter is to push the quantization noise from the quantizer out of the frequency band (or bands) of interest and afterwards filter the output signal y(n) in order to remove the quantization noise. In some applications (D/A converter or class-D amplifiers etc.) the post-filtering (decimation) of y(n) can be omitted, but this depends on the application where the sigma delta converter is used. The sigma delta converters have become very popular to use in recent years due to the modulation of the quantization noise property provided by the NTF function and the low cost to implement it.

MSA explanation

From the explanation from above it's clear that the loop filter H(z) should be designed with desired NTF properties in mind, i.e. the final NTF should be very aggressively with and high number of poles and zeros, i.e. with a wide stop-band, very good stop-band attenuation and a fast transition from the stop-band to the pass-band. Unfortunately, there is a limit to how aggressively the NTF can be. If this limit is exceeded the modulator will exhibit an unstable behaviour and it will simply start oscillating. In the following the stability of the modulator will be discussed.

For many years it was truly believed that it was impossible to design stable sigma delta modulators with higher order than two, mainly because of the highly nonlinear quantizer in the feedback path of the modulator.

This has since proven not to be true and many modulators of higher orders (i.e. a more aggressively NTF design) has been described in the literature over the last ten years. The linearized model of the modulator is also used for analyzing the stability of the modulators and many papers has been written about the stability problems and now several stability criteria has been developed where the most common ones are:

- The Gaussian stability criterion, the most popular
- The BIBO (bounded input -> bounded output) criterion
- The improved BIBO criterion

Common for all the stability criteria is that they all depend on the norm of the NTF functions described in the noise amplification factor A(Kn), i.e. from q(n) to y(n):

$$A(K_n) = \int_{-Fs/2}^{Fs/2} |NTF_{kn}(f)|_2^2 df = \|ntf_{Kn}(n)\|_2^2$$

The Gaussian is based on the two-norm (as in the equation above) and the BIBO is based on the one-norm, in the following only the Gaussian Criterion is explained. For higher orders modulators all A(Kn) curves are ∪convex curves. From the above it can be realized that the shape of the noise transfer function, implemented by the loop filter, plays an important role for the stability of the modulator.

Fig. 4 shows two different curves for the noise amplification factor A as a function of a linearized quantizer amplification factor Kn. The curves C1 and C2 are obtained for two different higher orders modulators with e.g. two 4^{th} order loop filters. The curves are ∪-convex curves, with a respective global minimum, Amin1 and Amin2, which exists between Kn = 0 and infinity.

Further it can be shown (please refer to the common literature) that the noise amplification curve, under the Gaussian quantization noise distribution assumption, also depends on the input level, m_x, of the modulator.

Fig. 5 shows a curve for the noise amplification factor A as a function of a signal peak value m_x for a Gaussian distributed quantizer input signal. This exemplary curve is shown for a 1-bit/two-level quantizer. It should be noted that the curve will be different for different number of levels. The curves are drawn up for a scale of numerical peak values between 0.0 and 1.0, where 1.0 represents a full-scale value.

The curves are drawn up from the following expression which represents the shown interdependency between the peak value m_x and the noise amplification factor $A(m_x)$

$$A(m_x) = \frac{1-m_x^2}{1-m_x^2-\frac{2}{\pi}\exp\left[-2\left(erf^{-1}(m_x)\right)^2\right]},$$

wherein erf() is the error function.

Here the input level m_x are assumed to be peak level of the input signal (actually a DC level is assumed because the Clock frequency Fs are much higher than the frequency of the signal: Fs >> Fsignal), please note that $A(m_x)$ curves for 3,4,.., N levels also exist.

As shown above, the noise amplification factor A depends on k_n and m_x i.e. as described by $A(k_n)$ and $A(m_x)$ in combination. A(Kn) and $A(m_x)$ are used to determine the unknown K_n gain factor for a given input level m_x of the modulator as described in the below.

Fig. 6 shows a relation between A(Kn) and A(m_x), quantizer gain Kn and a stable input range, MSA.

The stable sigma delta modulator will always follows these curves and from the curves it's possible to find the maximum stable input level, called the MSA, that assure that the modulator exhibit a stable behaviour. If the amplitude exceeds this input signal peak value (MSA) the modulator would potentially starts to oscillate and become unstable. Please note that the if the Amin point in the A(Kn) curve is greater than the A(m_x=0) point, then the modulator will be come unstable even for zero input signal. In figure 7 the stable input range for a third order Butterworth high-pass NTF function is sketched out.

From the explanation above it follows that the NTF function determines the Amin point which determine the achievable MSA, the smaller Amin the higher MSA. It can be shown from the A(Kn) function that the Amin points depends on the area under the |NTF| function, more area means a lower Amin and therefore a higher MSA, less area means higher Amin meaning a lower MSA. Again, since the area under the |NTF| curve is determined by the NTF filters stop bandwidth and transition bandwidth , a small stop-band (which always is desirable due to the quantization noise suppression) means a lower MSA.

Fig. 19 shows two examples of different NTF amplitude responses. The A and B curve emphasizes that the area under the NTF curve is an important parameter for the final noise contribution in the frequency band of interest.

It would always be desirable to have a high MSA, equal 1.0 and at the same time achieve a high suppression of the quantization noise when low input signal is applied to the modulator, and since these two wishes are conflicting

there is a need for obtaining these features, and this is what the current invention is providing.

From the above paragraph of the modulator analysis it follows that the peak value mx must be below a certain limit called the MSA and there is a trade off between MSA and the quantization noise. From this it follows that the MSA should be adapted to the peak value mx in order to achieve the maximum dynamic range. The invention circumvents the above mentioned trade-off between noise suppression and maximum input signal determined by the MSA, by dynamically altering the NTF and thus the noise suppression and MSA.

Fig. 7a and 7b shows the generic modulator with a generic control circuit that controls the NTF and STF of the modulator.

Noise shaping control (NSCTR) block explanation

The basic idea behind the invention is to actively control the loop filter H(z) (which again control the NTF) of the sigma delta modulator and thereby adjusts the MSA/Amin of the modulator to the input signal variations, or in other words an adaptive noise shaping controlled sigma delta converter.

The most general aspect of the invention is outlined in figure 7a and 7b. Here the m_x peak value is derived from the input or the output of the modulator (or both). The state variables inside the modulator i.e. the implementation of the H(z) rational polynomial also contain valuable information about the peak value this could also serve as an input to derive an estimate of the m_x value.

Fig. 8a, 8b and 8c shows different embodiments of the control circuit, NSCTR. The most general noise shaping control circuit is sketched out in figure 8a, and the control circuit consist of a peak detector which output serve as input to a NTF decision block. This block has to decide, based on the

estimated m_x value how the loop filter H(z) should be changed in order to achieve the wanted noise shaping properties. In this figure the peak detector has it's input from modulator input, modulator output or some of the state variables in the H(z) loop-filter. In fig. 8b a block diagram of preferred embodiment of the control block is sketched out, i.e the peak detector is based on a low-pass filter followed by double rectification and some lookup table logic that generates the control signals to the loop-filter H(z). Fig. 8c shows another preferred embodiment especially useful when the modulator is digital here the low-pass filter is omitted since the input is to the noise shaping CTR is taken from the digital input to the modulator. Please note that the rectification could be omitted and the signed peak value (or values) m_x could directly serve as input to the NTF decision block.

The peak detector could be implemented in many different ways, and the implemented signal properties of the detector would very much depend on the application. The phrase peak detect should be comprehended very broad, some examples are mentioned here:

- A detector that estimate the input signal;
- In some implementation the detector could be skipped and the input signal directly serve as an input to the NTF decision block;
- A peak detector with different release time and/or attack times, Especially the combination of "as close as possible to 0" attack time and different release time is interesting;
- A filtering device that divide the input signal into several frequency bands and then perform peak detections on each band. The outputs from each detector could be used as input to the NTF decision block.

The purpose of the NTF decision block is to control the loop filter H(z) in the sigma delta converter. Again, a lot of topologies exist in order to implement the NTF decision block:

- ROM based decision: The peak detector value is used to look up a set of coefficients in the H(z) rational polynomial.
- Instead of having a set of predefined polynomials, an algorithm based on the peak detector could actually make the changes to the coefficients in small steps, like the LMS algorithm.
- An additional polynomial could be inserted in parallel or serial with H(z) in order to shape the behaviour of the final H(z), again it's the peak detector output that control the behaviour of final H(z). Note that the order of the denominator in the final H(z) much always be greater than the numerator.

Examples of preferred embodiments

The preferred embodiment of the current invention depends of in which technology the modulators are implemented:

- Sigma delta modulator implemented in C-mos technology in a switch capacitor topology with an analogue signal input, i.e an analogue modulator;
- Sigma delta modulator implemented in C-mos technology with a digital input signal. i.e. digital modulator;
- Sigma delta modulator implemented on a general purpose CPU with a digital input signal, i.e. a software modulator;
- Sigma delta modulator implemented as a continuous time RC modulator.

The analogue modulator, preferred embodiment

Fig. 9 shows a block diagram of the adaptive, noise shaped controlled sigma delta converter when the modulator is implemented in a switch capacitor topology.

This topology is used if the input signal is analogue, i.e. continues in time and value. H(z) is implemented as a series of integrators in a 4'th order

modulator. In this figure all the e_i is zero if the modulator is the of the low-pass type, if the modulator is of the band-pass type the each pair of integrator along with e_i corresponds to a resonator.

The noise shaping control circuit, NSCTR, is preferably implemented as a digital circuit with input from the quantizer, but can also be implemented as an analogue circuit. It, NSCTR, provides an output which is a digital signal that controls a switch (or several switches) in the integrator H_i. Further, the gain k, feedback parameters b, and step size in the quantizer can be controlled. This is especially expedient for modulators with 3, 4 and higher number of levels.

The CTR consist of a peak detector which is used to lookup a set of digital control signals, these ON/Off signals is used to adjust the loop filter H(z) and thereby controlling the NTF of the modulator. Additionally, the gain k, feedback parameter b and the step size in the quantizer are also controllable.

In fig. 9 the peak detection value is double rectified in order to save logic in the lookup table, but the rectification could be omitted. Since the b-coefficients among others enable adjustment of the cut-off frequency of the NTF, they are preferably adjusted if it is desired to change MSA by changing the cut-off frequency fo of the NTF. Likewise, adjustment of the quantization step size enables change of the cut-off frequency.

Fig. 10a and 10b show block diagrams of the integrator $H_i(z)$ of the modulator. Each H_i in the figure is implemented as an integrator. The input to the block is an analogue signal (time discrete but continues in value) and the On/Off control signal (or several) from the NSCTR block. The On/Off control signal determine the value of f_i, in a switch capacitor implementation this is done by removing a specific amount of charge on the integrating capacitor of

the integrator in each clock period the CTR signal is On. The amount of charge that is removed corresponds to the value f_i and by having n control signals to each integrator it's possible to have 2^n different f_i value for each H_i block.

The main idea is this implementation is to add some loss to each integrator depending on the peak value of the signal. As the input signal peak value gets higher the more loss is added to the H_i integrators which will change the corresponding NTF function to a less aggressive high pass filter.

In these embodiments solutions is described whereln a losses in the integrators are used to change the NTF, but other solutions could also be used; e.g. changing the coefficients and/or changing the resolution of the quantizer, i.e. basically any parameter which changes the noise transfer function, NTF.

Simulations have been performed in connection with which several output spectrums from the modulator in fig. 9 is plotted for a 1 kHz sine wave but with different input amplitude. A 24 kHz low-pass filter is applied to the modulator output signal. The modulator runs running at 2.4 MHz clock frequency, and it's clearly shown that the quantization noise shaping provided by the NTF is changed according to the input amplitude and the wanted effect on the NTF is provided: Better noise shaping when small signals are applied, and the MSA of 1.0 is reached even though it's a 4'th order modulator.

Within the scope of the present invention different strategies for the control of an adaptive noise shaping is available. Fig. 11 through 14 illustrates four different examples of selecting one of three different noise transfer functions in response to a peak value or another signal feature e.g. the signal itself, a low-pass filtered signal or others. Here, only three different noise transfer

functions are shown as being selectable, however within the scope of the invention only two different noise transfer functions or four, five, six or even more noise transfer functions can be selectable. The number of selectable noise transfer functions depends on the one hand on the chip area or computational power available for providing filter coefficients to the loop filter and making a decision on which coefficients, and thus NTF, to select under the adaptive control and, on the other hand, how close to an optimum MSA it is desired to operate the sigma delta modulator. An optimum MSA and a suboptimum MSA is illustrated in fig. 18b.

Common for fig. 11 through 14 is that a fixed topology of 4^{th} or 3^{rd} order has been chosen and that a basic H(z) is with all zeros at DC i.e. the integrator type of modulator. In these examples two features of the NTF are changed:

- The high-pass cut-off frequency fo of the NTF;
- Some loss is added to the integrator to lower the amplification of H(z) at DC. This gives a less steep amplitude response curve for the NTF characteristic and therefore exhibits a lower order characteristic.

From the below four figures it is clear that the noise shaping of the modulator is adapted stepwise to an amplitude of a signal in the sigma delta modulator.

Fig. 11 shows a first set of noise transfer functions that provides different MSA values and different quantization noise attenuation.

Fig. 12 shows a second set of noise transfer functions that provides different MSA values and different quantization noise attenuation.

Fig. 13 shows a third set of noise transfer functions that provides different MSA values and different quantization noise attenuation.

Fig. 14 shows a fourth set of noise transfer functions that provides different MSA values and different quantization noise attenuation.

The digital modulator, preferred embodiment

Fig. 15 shows another preferred embodiment of the sigma delta converter according to the invention when implemented as a digital modulator. Even though that the modulator sketched out in fig. 9, is the preferred embodiment when an analogue implementation is used, it could also serve as an embodiment for a digital implementation of the digital modulator. But since the f_i value in the integrators H_i in general are real values between 0 and 1 it require a multi-bit multiplication with the multi-bit integrator output and this is not very feasible. A better embodiment for a digital implementation is sketched out in figure 16 here the output from the lookup table in the NTF CTR block directly control the "b" feedback coefficients and the multiplication is avoided and each integrator H_i are implemented as in figure 16a.

Please also note that the input to the NTF CTR block is taken from the input to the modulator and there is no need for the low-pass filter. Please note that all the "a" coefficients has been removed again due to avoid the multiplication and also the "e" coefficients have been removed because the modulator is of the low-pass type, but the e coefficients has to be taken into account if a band-pass type of modulator is implemented at the cost of two multiplier. Please also note that the feedback coefficient b of the first integrator is '1' since all the coefficient has been scaled with the b1 coefficients.

Fig. 16a and **16b** show block diagrams of the integrator $H_i(z)$ of the modulator in fig. 15.

Fig. 17 shows another preferred embodiment of a digital modulator. The difference to the analogue implementation is that the integrator in figure 17 is restricted to the f_i value: $f_i = 1/2n$ n=-0, -1, -2, -3....., this restriction will avoid

the multiplications. By adding these losses in the integrator it's possible to add some zero's in the NTF functions and the noise shaping will exhibit lower order noise shaping.

Fig. 18a shows a range of required MSA for a given input signal peak value to provide stable operating conditions. A plot of an optimum MSA versus the peak value is provided in the form of the straight line. The hatched area represents the range of required MSA for a given input signal peak value to provide stable operating conditions.

Fig. 18b shows a realized MSA as a function of a input signal peak value, mx, for an exemplary design in which the MSA can be adapted to the peak value by selecting of one of five different noise transfer functions. In practical embodiments it is very difficult to control the loop filter H(z) in order to achieve the optimum MSA/mx line in fig. 18a and a sub-optimum, but practical solution is shown in fig. 18b, where the MSA is achieved by adapting to a measured mx value in discrete steps. This means that a final set of loop-filters can be implemented.

Fig. 19 shows different noise levels in a frequency band of interest.

The software modulator

In this implementation a general purpose CPU is used to implement the modulator, here the input signal to the modulator would be digital signal. But since a general CPU typical has a build in multiplier and the power consumption are less restrictive, there will be other priority than in the digital implementation. Which means the block diagram from the analogue or digital or a mix, could be used as a block diagram of the preferred embodiment for this modulator.

CLASS-D AMPLIFIER APPLICATION

The modulator can also, with great advantage, be used in a Class D amplifier. Class D has in recent years become very popular as they have very high power efficiency, are compatible with mainstream inexpensive CMOS technology and can be made with very high performance on a very small silicon die area. The simplest form of a class D amplifier comprises a modulator and a so called H-Bridge.

Fig. 20 shows a class-D amplifier comprising a sigma delta modulator and a H-bridge arranged to drive a load. The class-D amplifier comprises a sigma delta modulator, a H-Bridge and a speaker. A Sigma Delta modulator is used to convert the input signal into a pulse density signal as input for the H-Bridge. Other types of modulators can also be used but here we will focus on sigma delta modulators as this relates directly to the invention. Also we have focused on two level modulators but it can be extended to higher level modulators e.g. 3, 4 or 5 levels or even more levels.

The function of the H-Bridge is to connect the load, which in this case is a speaker to either VDD-GND or GND-VDD. This represents the two outputs of the Sigma Delta modulator i.e. +1 and -1, in the case of a two level modulator. The load will then be exposed to a wide band signal consisting both of the desired low frequency signal and the high frequency quantization noise. As the speaker itself has a low-pass filter frequency response, it will by itself do the decimation, that is, to filter out undesired high-frequency signals. The filter effect of the loudspeaker is generally well-known.

The sigma delta modulator applied in the class-D amplifier is subject to the stability criteria mentioned above. Thus, the amplifier i.e. the modulator is to be operated to adapt its MSA, by selecting an appropriate loop filter characteristic, to obtain a maximum suppression of quantization noise for a measured input signal amplitude.

To obtain the largest possible dynamic range the MSA should normally be designed for approx 0.5. This has the consequence that the maximum output signal is 6dB lower than what can be achieved if the MSA was equal to one. Or one is forced to increase the noise to unacceptable levels in order to increase the MSA. This is the reason why the use of sigma delta modulators has not become so popular for Class D amplifiers, despite the fact that they are very simple to implement. These short-comings related to class-D amplifiers are overcome by the present invention.

The invention allows an optimization of the adaptive behaviour under which a relatively aggressive suppression of the quantization noise is applied when relatively low signal amplitudes are detected, whereas when relatively high signal amplitudes are detected, a less aggressive suppression of the quantization noise is applied.

In class-D amplifiers for audio use the invention is especially advantageous as the ear is very sensitive to noise at low signal levels, whereas the ear will be less sensitive to noise at high signal levels. This property is referred to as masking i.e. a relatively high-level audio signal will mask noise such that a present relatively high noise level is not perceived as dominantly as it would be for relatively low-level audio signals.

Fig. 21 shows a configuration of an H-bridge. An H-Bridge in its simplest form comprises four switches in the figure denoted Sw1-P1 to Sw4-p1. Two of them connected to VDD (Sw1-p1 and Sw3-p2) and two connected to GND (Sw2-p2 and Sw4-p1).

By controlling these switches the output load, which can be a speaker, can be connected to VDD at one of its two terminals and GND at the other thereby generating a voltage corresponding to a logic +1. In the same way a -1 can be generated, i.e. +1*Vdd and -1*Vdd.

Control signals for generating a series of -1,+1,-1 is shown as P1 and P2, i.e. the signal P1 controls switches Sw1-p1 and Sw4-p1 and P2 controls the switches Sw2-p2 and Sw4p1.

The H-Bridge can easily be extended to three levels. By connecting both sides of the speaker to either GND or VDD a zero can be generated. A control circuit for the switches are trivial to implement and will not be shown here.

MICROPHONE APPLICATION

Fig. 22 shows a first embodiment of a digital microphone. In this aspect of the invention, the digital microphone 901 comprises an integrated circuit 902 with a microphone voltage bias circuit 903, 904; an amplifier 905 with a transfer characteristic which suppresses spectral components below an audio band and provides a substantial flat frequency response for audio frequencies at a nominal gain; an anti-aliasing filter 906 and a sigma-delta converter 907. The integrated circuit 902 comprises terminals Tc1, Tc2, Tc3, Tc4 for coupling to the microphone element 908, the bias voltage, a ground reference potential and a supply voltage, respectively. Terminal Tc6 provides a digital signal from the A/D converter and via terminal Tc5 a clock signal is provided to the A/D converter. The supply voltage to the amplifier 905 and the sigma-delta converter can be provided via the terminal Tc6, in which case the terminal Tc4 can be omitted.

Fig. 23 shows a second embodiment of a digital microphone. In this aspect of the invention, the digital microphone 1001 comprises an integrated circuit 1002 with a DC voltage regulator 1003 which provides a regulated voltage to the amplifier 1009 and the sigma-delta converter 1011. The microphone bias voltage is provided by an on-chip voltage up-converter 1004 which receives

an off-chip oscillating signal with a voltage amplitude; in response thereto the up-converter provides an output oscillating signal with a larger voltage amplitude. This output signal is low pass filtered by low pass filter 1005 and provided via a series resistor 1006 to the microphone element 1008. A capacitor 1007 blocks the DC bias voltage from the input of the amplifier 1009 with the transfer function mentioned above. Output of the amplifier 1009 is provided to an anti-aliasing filter 1010 before being input to a sigma-delta converter 1011.

The voltage up-converter or voltage pump, UPC, 1004 can be in the form of a so-called Dickson-converter. The voltage pump is operated by an oscillator which preferably provides a square-wave oscillator signal to the voltage pump. Other signals, eg sine waves or filtered square waves, with lower contents of harmonics may be used to obtain lower noise. As an alternative, the oscillator can be embedded on the chip 1002.

It is shown that the up-converter and the sigma delta converter shares the same oscillator/clock signal as provided via terminal Tc4. It should be noted that the signal may be divided to obtain different oscillating/clock signal frequencies to the UPC and sigma-delta converter.

Fig. 24 shows a block diagram of a digital microphone.

Fig. 25 shows another block diagram of a digital microphone. Here, a buffer or buffer amplifier is inserted before the sigma-delta converter.

Fig. 26 is a schematic view of a microphone with an integrated circuit and a microphone member. The microphone is shown as a cartridge with a microphone member, comprising the microphone membrane and an integrated circuit.

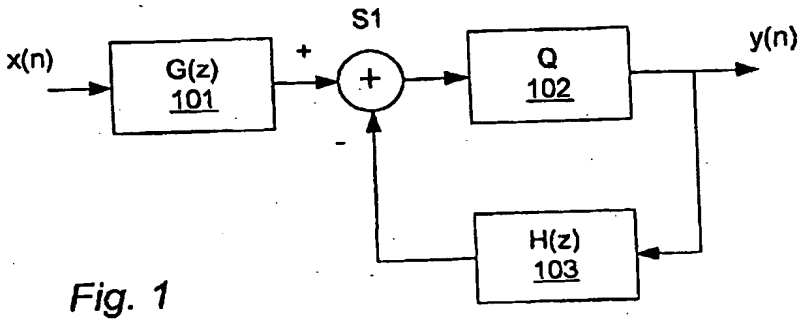


Fig. 1

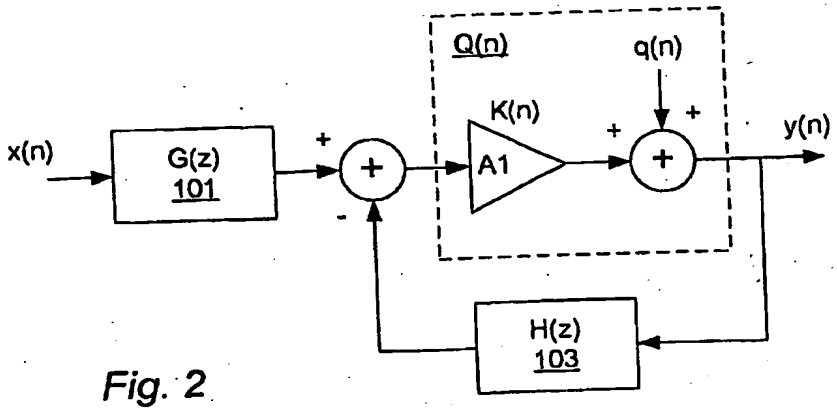


Fig. 2

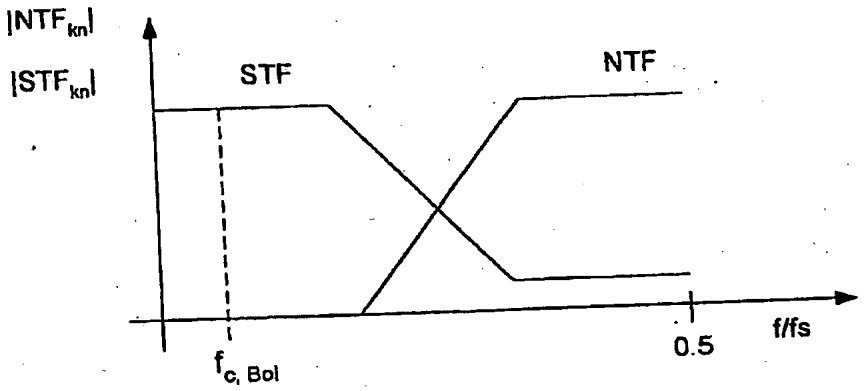


Fig. 3

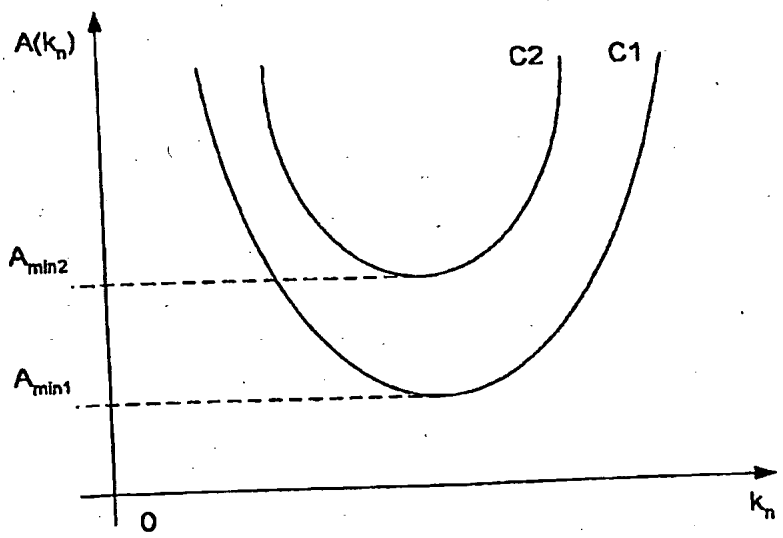


Fig. 4

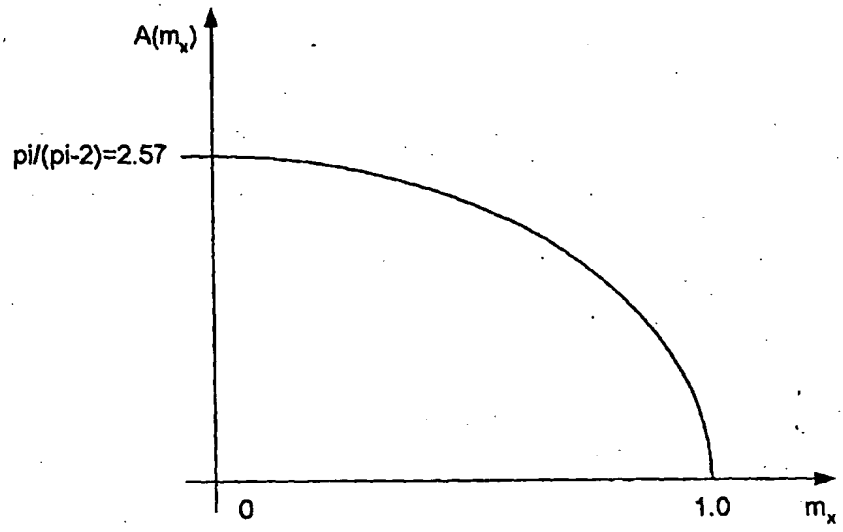


Fig. 5

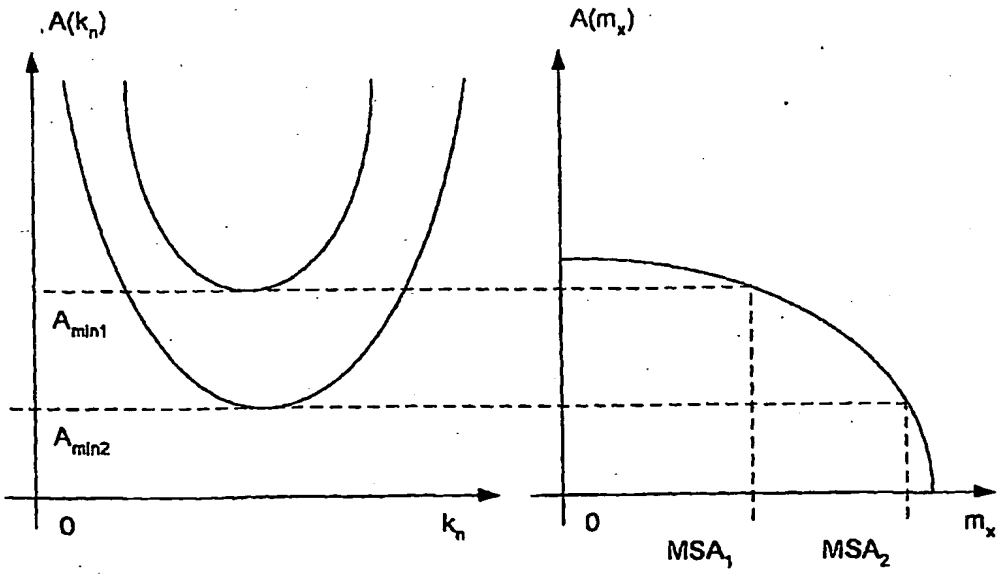


Fig. 6

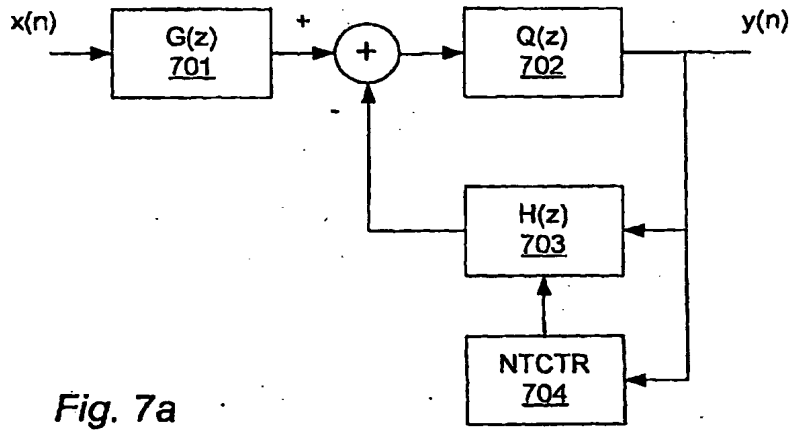


Fig. 7a

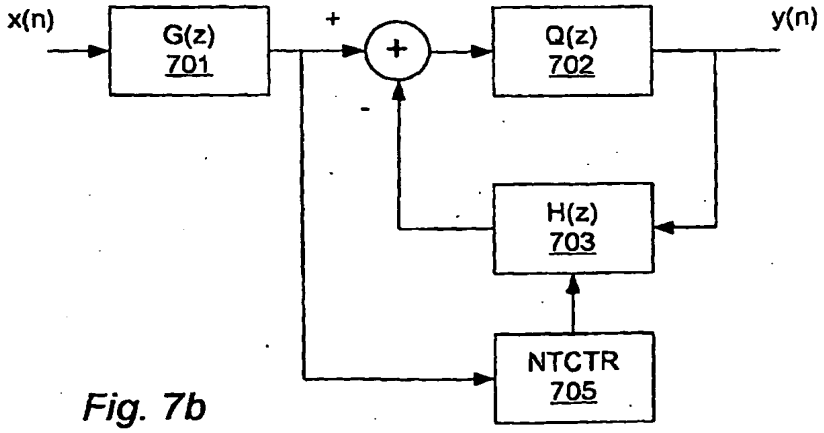


Fig. 7b

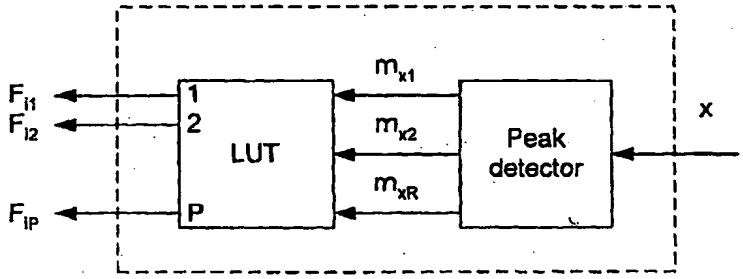


Fig. 8a

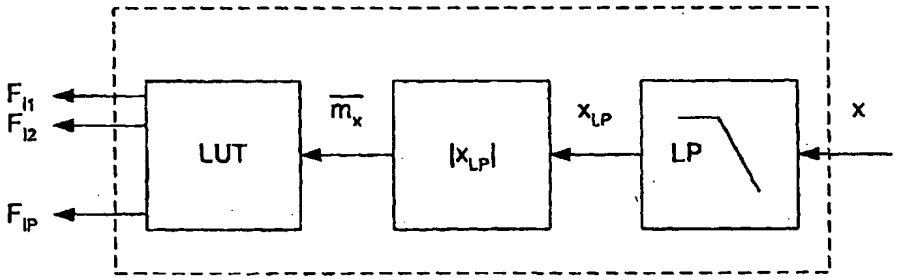


Fig. 8b

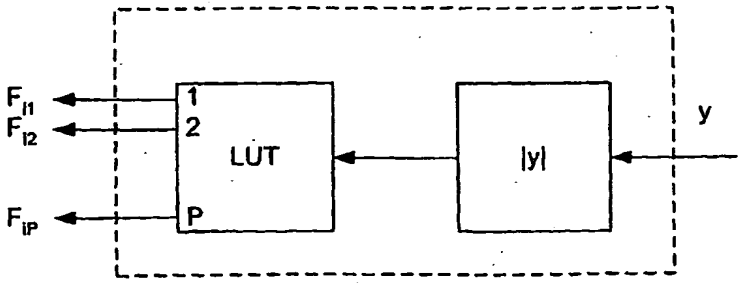


Fig. 8c

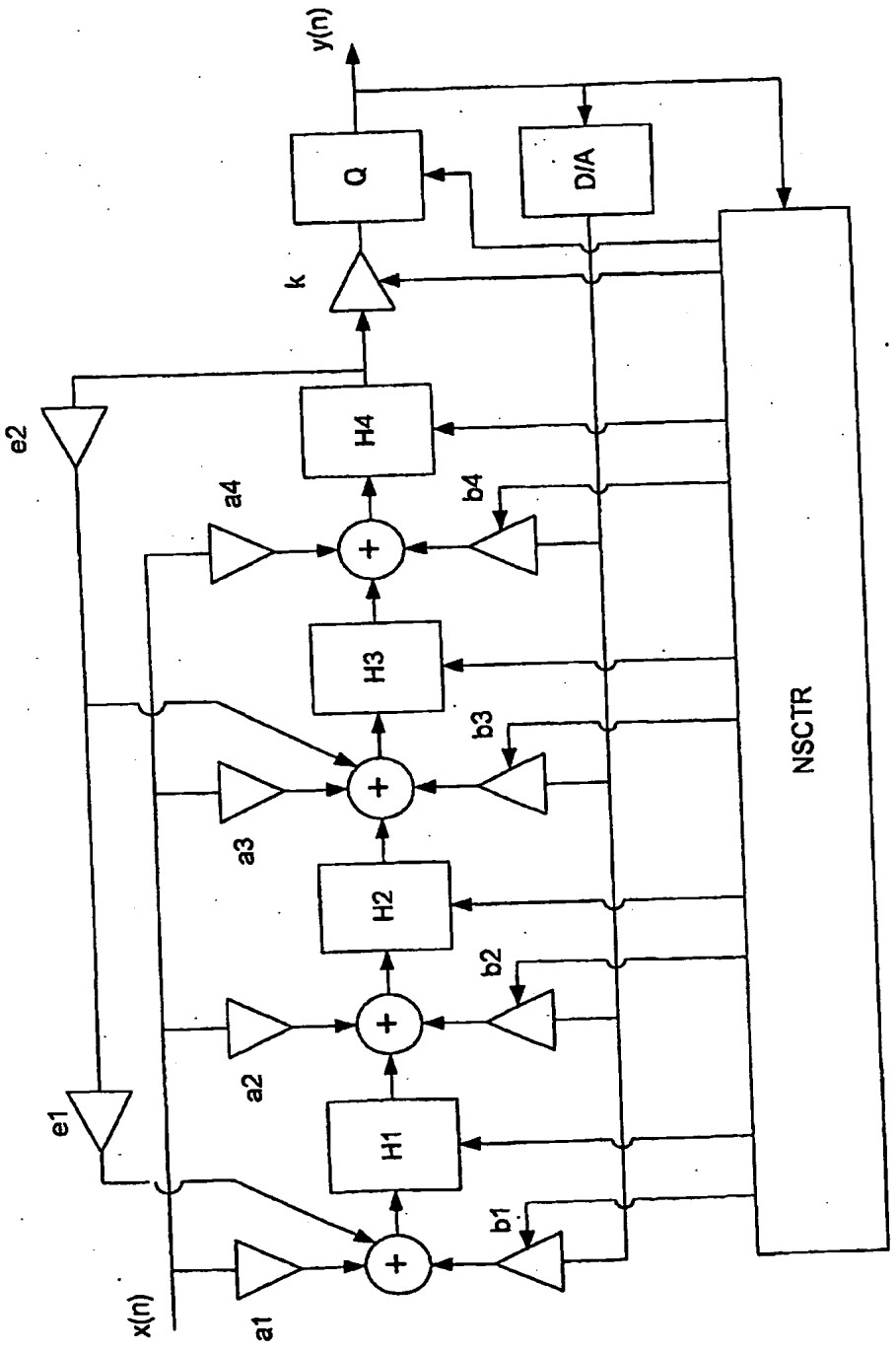


Fig. 9

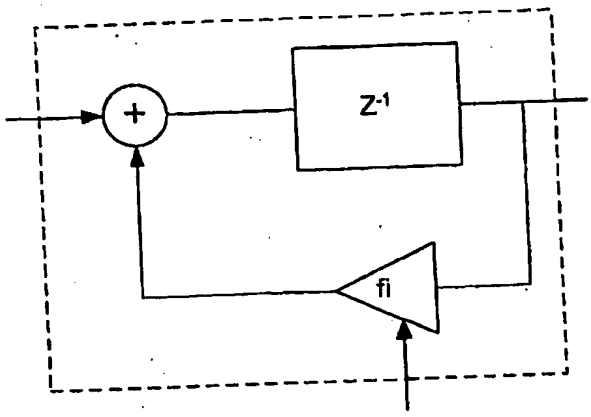


Fig. 10a

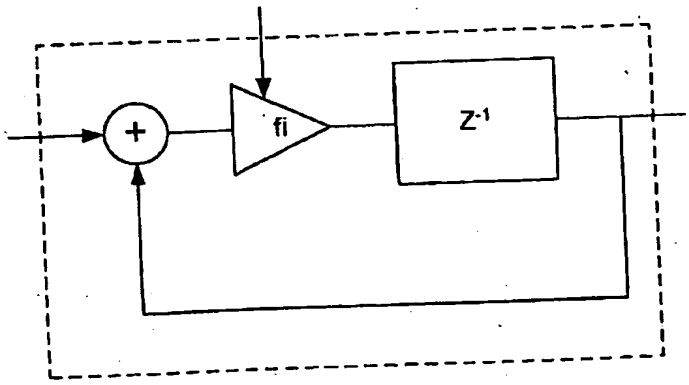
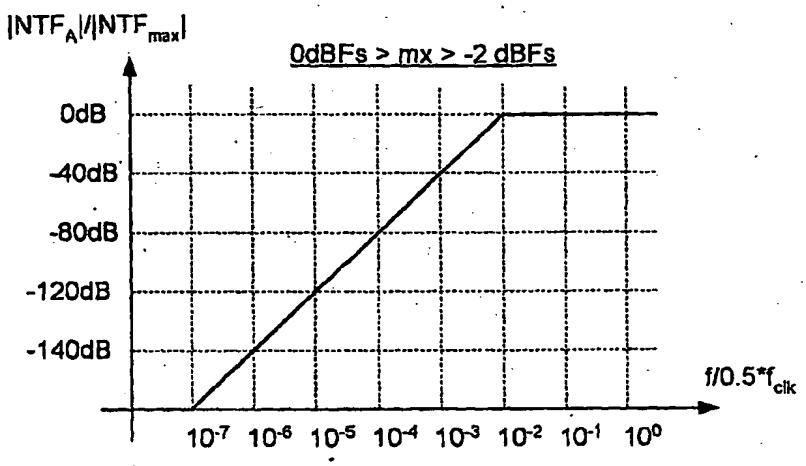
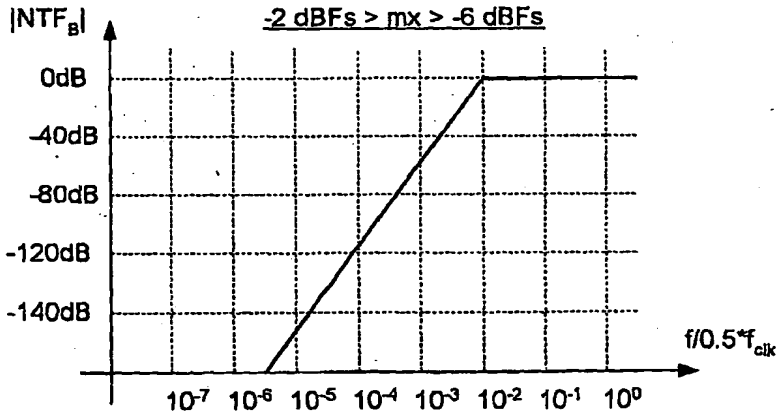


Fig. 10b

2nd order NTF adaption



3rd order NTF adaption



4th order NTF adaption

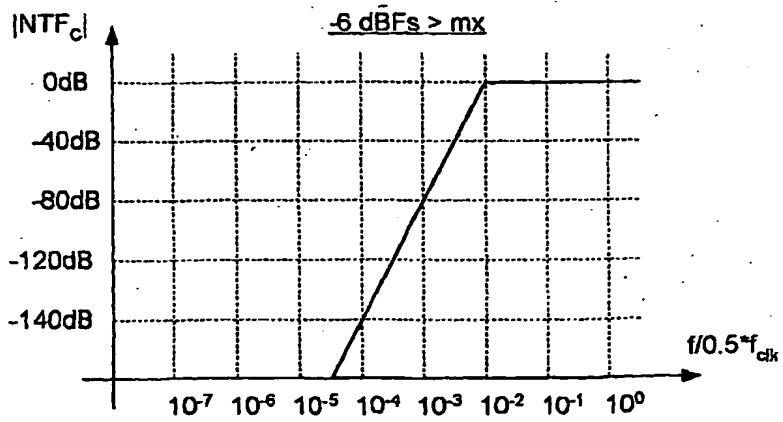
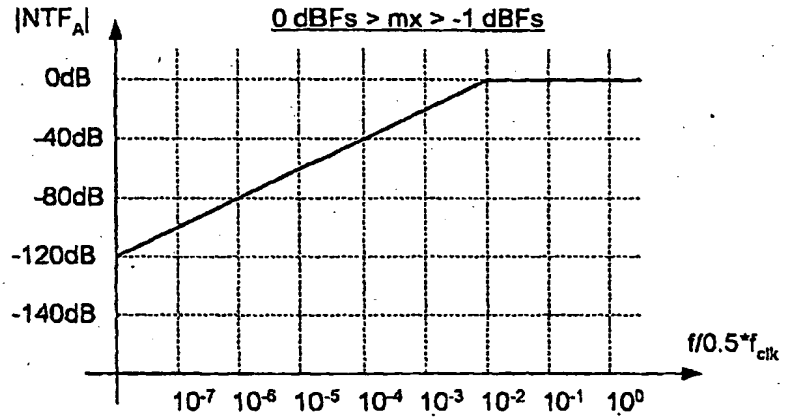
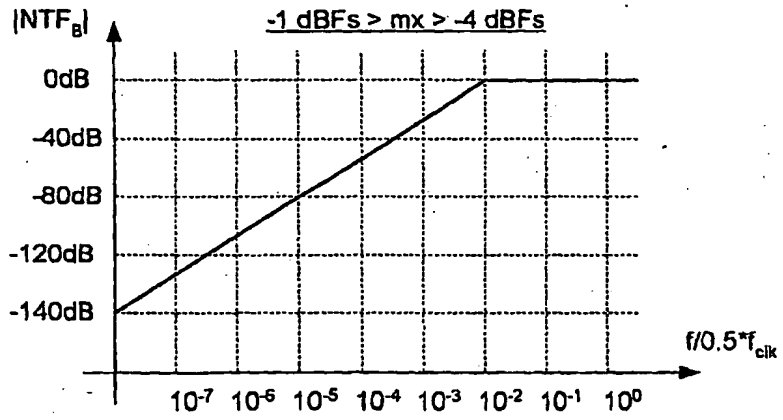


Fig. 11

1st order NTF adaption



2nd order NTF adaption



3rd order NTF adaption

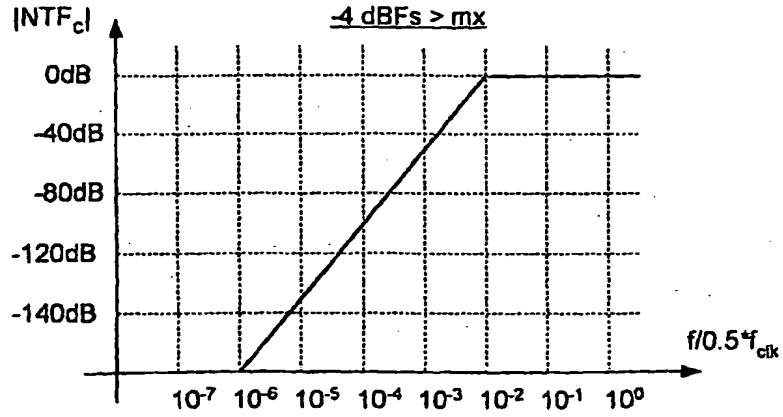
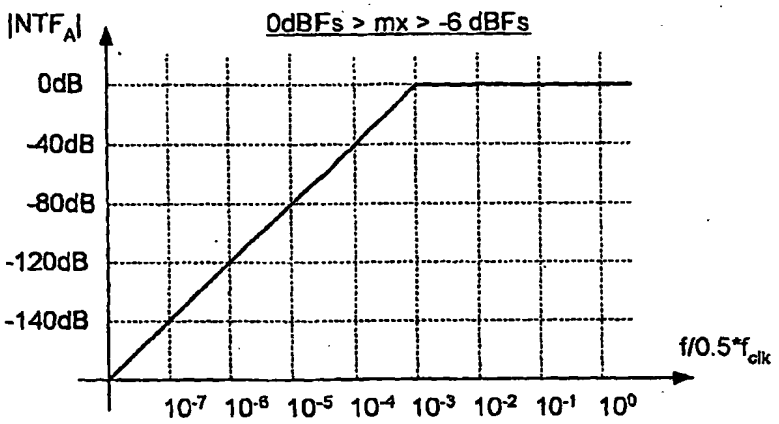


Fig. 12

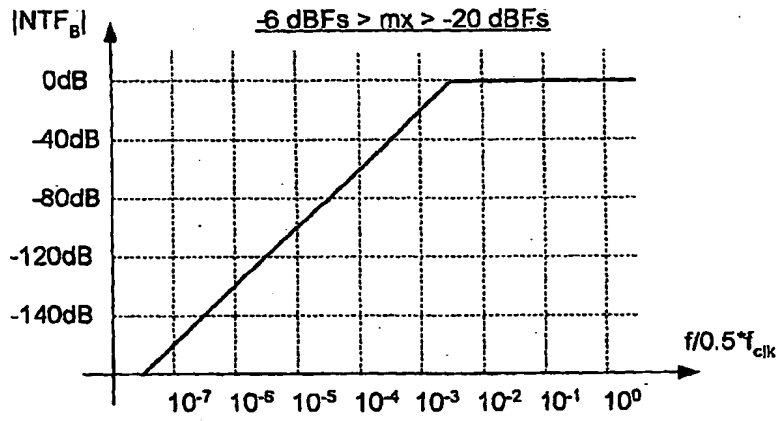
2nd order NTF adaption

fo=10^{-3}



2nd order NTF adaption

fo=$1.3*10^{-3}$



3rd order NTF adaption

fo=$1.9*10^{-1}$

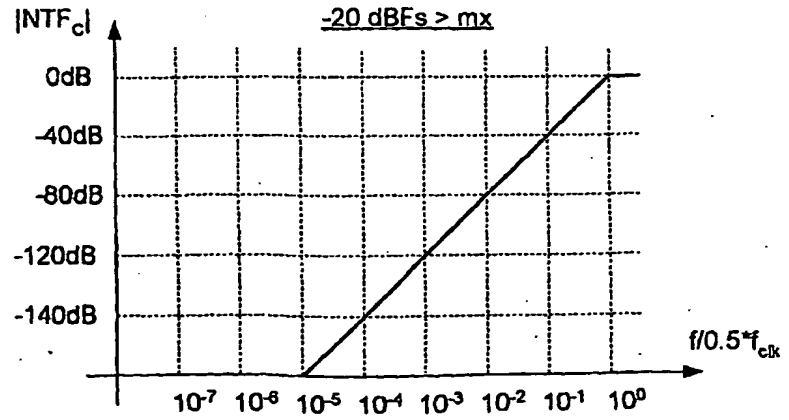
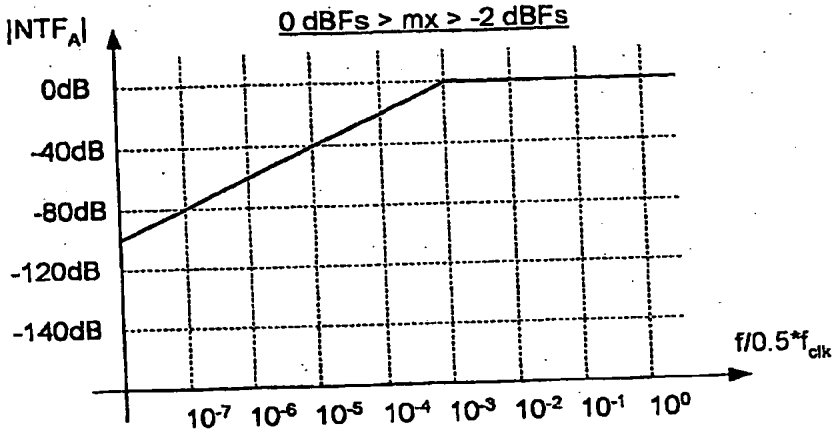


Fig. 13

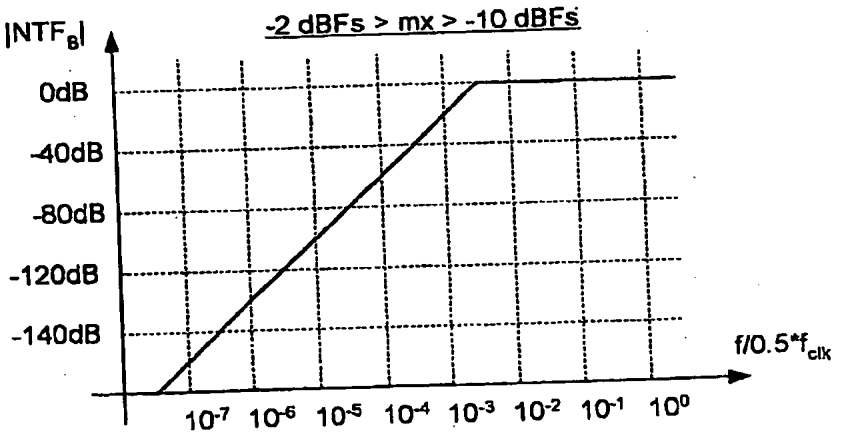
1st order NTF adaption

$f_o=10^{-3}$



2nd order NTF adaption

$f_o=1.3*10^{-3}$



4th order NTF adaption

$f_o=10^{-1}$

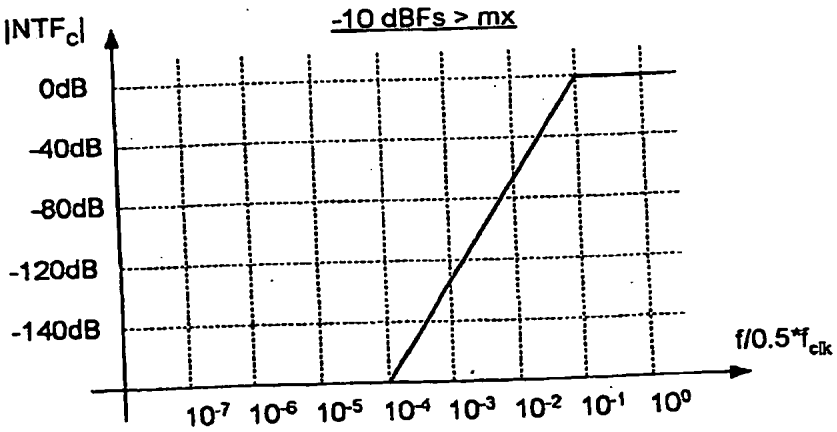


Fig. 14

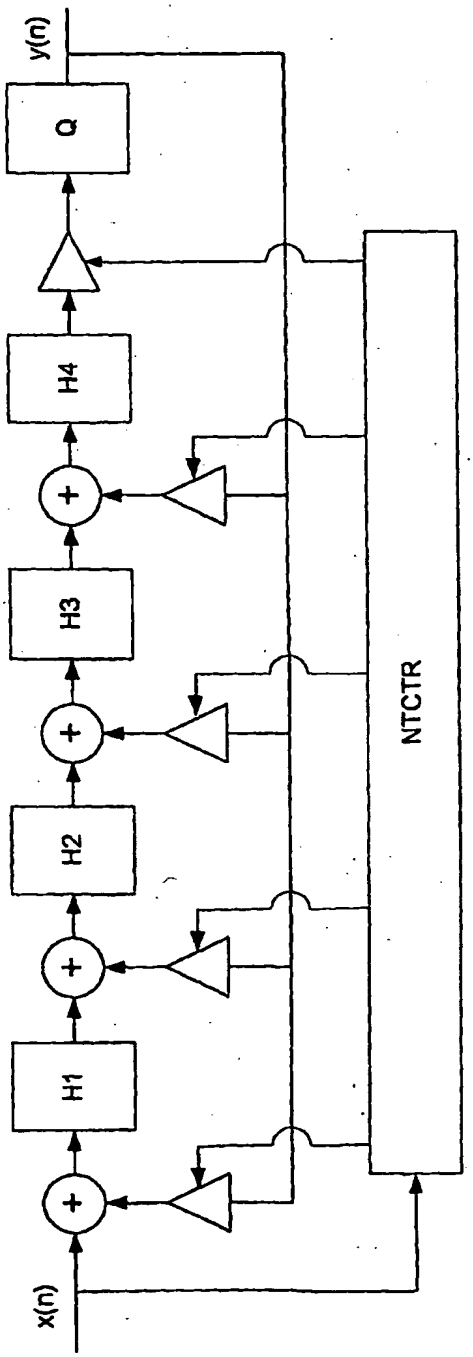


Fig. 15

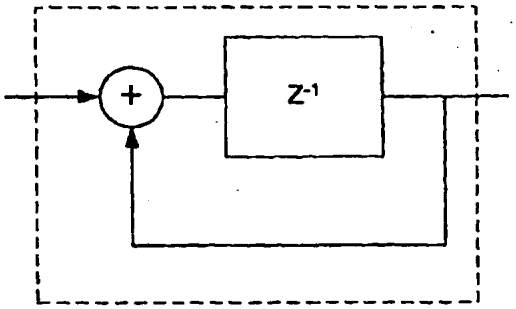


Fig. 16a

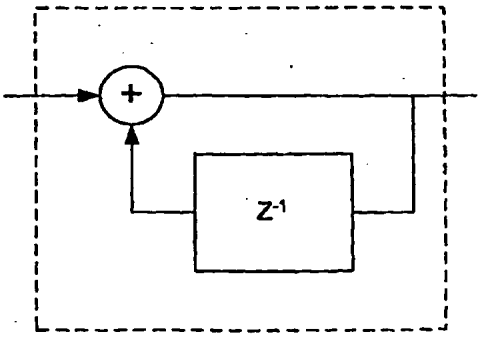


Fig. 16b

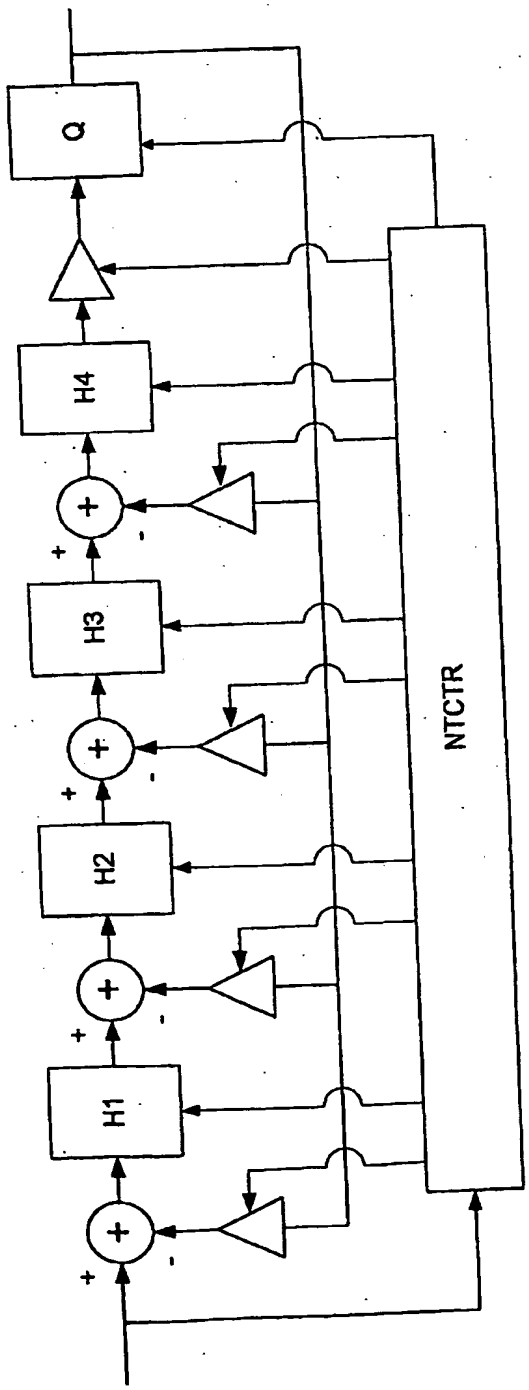


Fig. 17

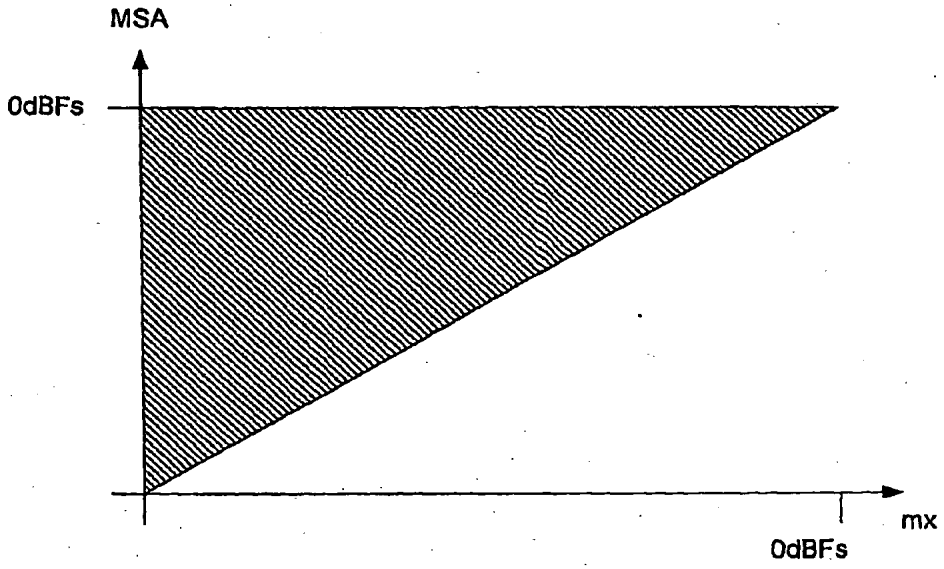


Fig. 18a

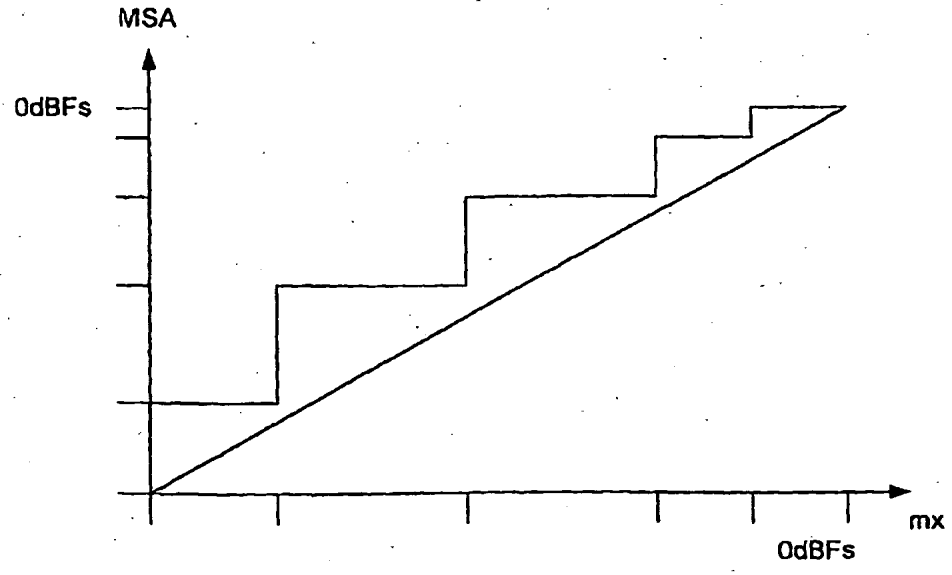


Fig. 18b

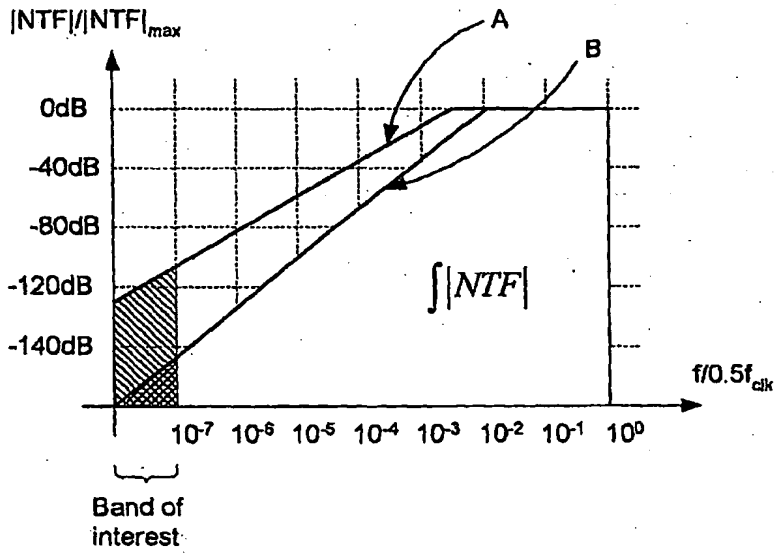


Fig. 19

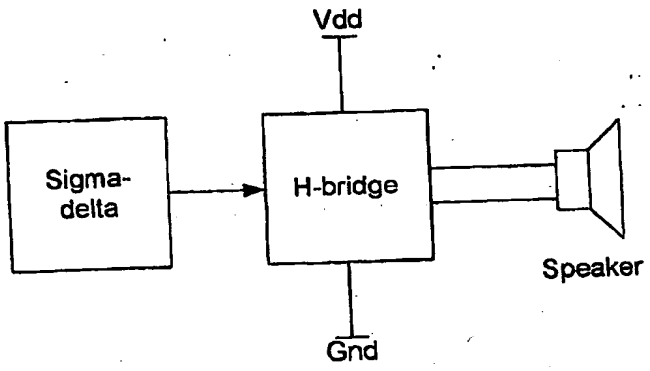


Fig. 20

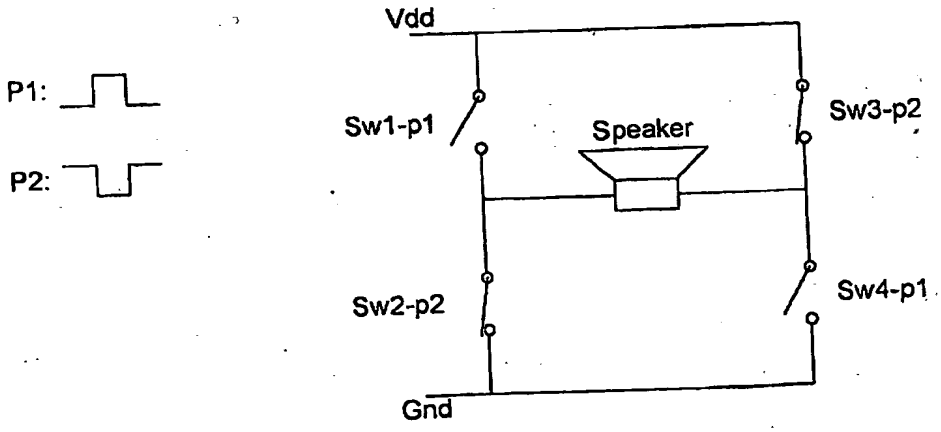


Fig. 21

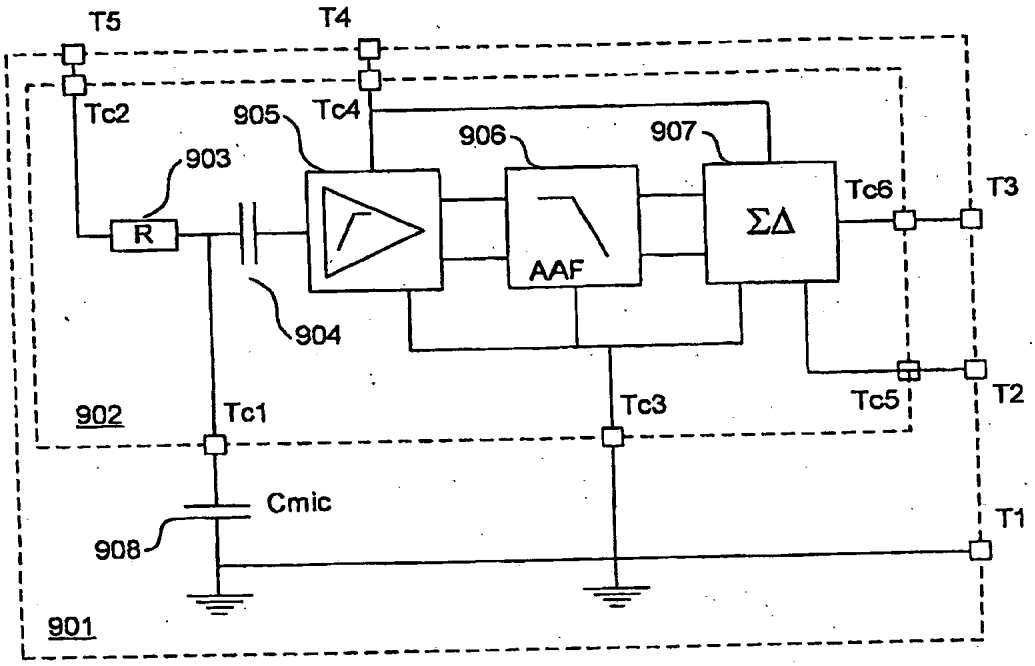


Fig. 22

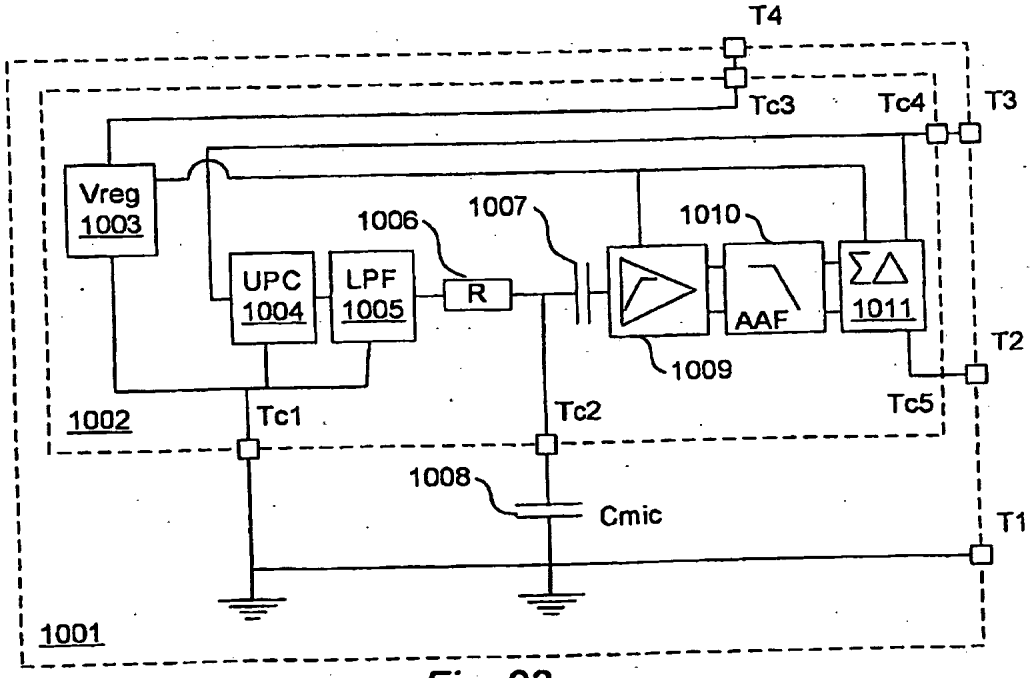


Fig. 23

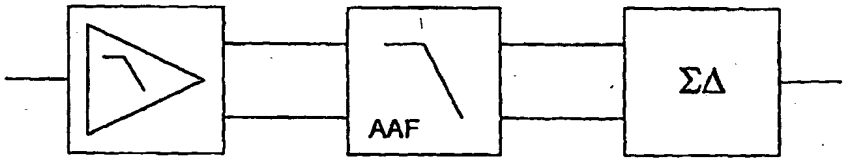


Fig. 24

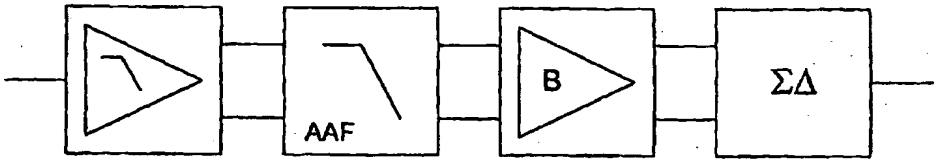


Fig. 25

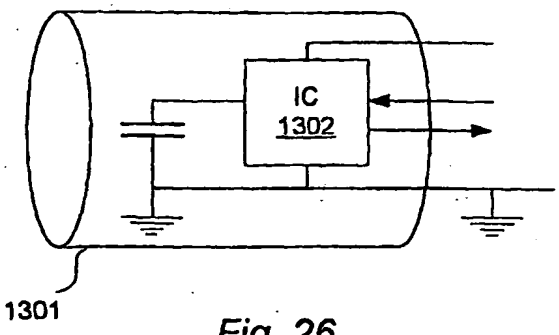


Fig. 26